IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A non-volatile semiconductor memory device, comprising:

a semiconductor substrate;

first and second semiconductor regions of a first conductivity type formed in said semiconductor substrate;

a first channel region and a second channel region between said first semiconductor region and said second semiconductor region in said semiconductor substrate, said first channel region being located on the side close to said first semiconductor region and said second channel region being located on the side close to said second semiconductor region;

a first gate formed above said first channel region via a first insulator; and

a second gate formed above said second channel region via a second insulator,

wherein writing and erasing operations are performed by injecting electric charge into said second insulator, and

the charge density of an impurity in said first channel region is different from the charge density of an impurity in said second channel region.

2. (Original) The non-volatile semiconductor memory device according to claim 1,

wherein the charge density of an impurity in said second channel region is lower than the charge density of an impurity in said first channel region.

3. (Original) The non-volatile semiconductor memory device according to claim 1,

wherein the impurity of a second conductivity type opposite to said first conductivity type is introduced into said first channel region, and the impurity of the first conductivity type and the impurity of the second conductivity type are introduced into said second channel region.

4. (Original) The non-volatile semiconductor memory device according to claim 1,

wherein said second insulator is a laminated film of a 10 silicon oxide film, a silicon nitride film, and a silicon oxide film.

5. (Original) The non-volatile semiconductor memory device according to claim 1,

wherein the thickness of said second insulator is larger than the thickness of said first insulator.

6. (Original) The non-volatile semiconductor memory device according to claim 1,

wherein the charge density of an impurity in said second channel region is set within the range of $10^{17}/cm^3$ to $10^{18}/cm^3$.

7. (Original) The non-volatile semiconductor memory device according to claim 1,

wherein said second gate is adjacent to said first gate via said second insulator.

8. (Original) The non-volatile semiconductor memory device according to claim 1,

wherein said second insulator has a charge holding function, the writing operation is performed by injecting electrons into said second insulator, and the erasing operation is performed by injecting holes into said second insulator.

9. (Original) A non-volatile semiconductor memory device, comprising:

a semiconductor substrate;

first and second semiconductor regions of a first conductivity type formed in said semiconductor substrate;

a first channel region and a second channel region between said first semiconductor region and said second semiconductor region in said semiconductor substrate, said first channel region being located on the side close to said first semiconductor region and said second channel region being located on the side close to said second semiconductor region;

a first gate formed above said first channel region via a first insulator; and

a second gate formed above said second channel region via a second insulator,

wherein writing and erasing operations are performed by injecting electric charge into said second insulator,

said second channel region includes a first region on the side close to said second semiconductor region and a second region on the side close to said first channel region, and the charge density of an impurity in said first region is higher than the charge density of an impurity in said second region.

10. (Original) The non-volatile semiconductor memory device according to claim 9,

wherein the impurity concentration of the second conductivity type opposite to said first conductivity type of said first region is higher than the impurity concentration of the second conductivity type of said second region.

11. (Original) The non-volatile semiconductor memory device according to claim 9,

wherein the impurity of the second conductivity type opposite to said first conductivity type is introduced into said first channel region, the impurity of the first conductivity type and the impurity of the second conductivity type are introduced into said second channel region, and the impurity concentration of the second conductivity type of said first region is higher than the impurity concentration of the second conductivity type of said second region.

12. (Original) The non-volatile semiconductor memory device according to claim 9,

wherein said second insulator is a laminated film of a silicon oxide film, a silicon nitride film, and a silicon oxide film.

13. (Original) The non-volatile semiconductor memory device according to claim 9,

wherein the charge density of an impurity in said first channel region is higher than the charge density of an impurity in said second region.

14. (Original) The non-volatile semiconductor memory device according to claim 9,

wherein said second gate is adjacent to said first gate via said second insulator.

15. (Original) The non-volatile semiconductor memory device according to claim 9,

wherein said second insulator has a charge holding function, the writing operation is performed by injecting electrons into said second insulator, and the erasing operation is performed by injecting holes into said second insulator.

16. (Original) A non-volatile semiconductor memory device, comprising:

a semiconductor substrate;

first and second semiconductor regions of a first conductivity type formed in said semiconductor substrate;

a first channel region and a second channel region between said first semiconductor region and said second semiconductor region in said semiconductor substrate, said first channel region being located on the side close to said

first semiconductor region and said second channel region being located on the side close to said second semiconductor region;

a first gate formed above said first channel region via a first insulator; and

a second gate formed above said second channel region via a second insulator,

wherein writing and erasing operations are performed by injecting electric charge into said second insulator, and

the charge density of an impurity in said second channel region is set within the range of $10^{17}/cm^3$ to $10^{18}/cm^3$.

17. (Original) A non-volatile semiconductor memory device, comprising:

a semiconductor substrate;

first and second semiconductor regions of a first conductivity type formed in said semiconductor substrate;

a first channel region and a second channel region between said first semiconductor region and said second semiconductor region in said semiconductor substrate, said first channel region being located on the side close to said

first semiconductor region and said second channel region being located on the side close to said second semiconductor region;

a first gate formed above said first channel region via a first insulator; and

a second gate formed above said second channel region via 15 a second insulator,

wherein writing and erasing operations are performed by injecting electric charge into said second insulator, and

when injecting holes into said second insulator, voltage pulse for injecting holes into said second insulator is applied

several times to said second gate and said second semiconductor region.

18. (Original) The non-volatile semiconductor memory device according to claim 17,

wherein said voltage pulse applies negative potential to said second gate and applies positive potential to said second semiconductor region.

19. (Original) A non-volatile semiconductor memory device, comprising:

a semiconductor substrate;

first and second semiconductor regions of a first conductivity type formed in said semiconductor substrate;

a first channel region and a second channel region between said first semiconductor region and said second

semiconductor region in said semiconductor substrate, said first channel region being located on the side close to said first semiconductor region and said second channel region being located on the side close to said second semiconductor region;

a first gate formed above said first channel region via a first insulator; and

a second gate formed above said second channel region via a second insulator,

wherein writing and erasing operations are performed by injecting electric charge into said second insulator, and

when injecting holes into said second insulator by applying first voltage pulse which applies negative potential to said second gate and applies positive potential to said second semiconductor region, second voltage pulse for applying positive potential to said second gate electrode is applied before applying said first voltage pulse.

20. (Original) A non-volatile semiconductor memory device, comprising:

a semiconductor substrate;

first and second semiconductor regions of a first conductivity type formed in said semiconductor substrate;

a first channel region and a second channel region between said first semiconductor region and said second semiconductor region in said semiconductor substrate, said first channel region being located on the side close to said first semiconductor region and said second channel region being located on the side close to said second semiconductor region;

a first gate formed above said first channel region via a first insulator; and

a second gate formed above said second channel region via a second insulator,

wherein writing and erasing operations are performed by injecting electric charge into said second insulator, and

after injecting holes into said second insulator by applying first voltage pulse which applies negative potential to said second gate and applies positive potential to said second semiconductor region, second voltage pulse which applies negative potential to said second gate electrode and applies ground potential to said second semiconductor region is applied.

21. (Original) A non-volatile semiconductor memory device, comprising:

a semiconductor substrate;

first and second semiconductor regions of a first conductivity type formed in said semiconductor substrate;

a first channel region and a second channel region between said first semiconductor region and said second semiconductor region in said semiconductor substrate, said first channel region being located on the side close to said first semiconductor region and said second channel region being located on the side close to said second semiconductor region;

a first gate formed above said first channel region via a first insulator; and

a second gate formed above said second channel region via a second insulator,

wherein writing and erasing operations are performed by injecting electric charge into said second insulator,

when injecting electrons into said second insulator, potential higher than that of said first semiconductor region is applied to said second semiconductor region and potential higher than that of said second semiconductor region is applied to said second gate,

when injecting holes into said second insulator, potential lower than that of said second semiconductor region is applied to said second gate, and

when reading data of the charge injected into said second insulator, potential higher then that of said first semiconductor region is applied to said second semiconductor region.

22. – 29. (Cancelled)